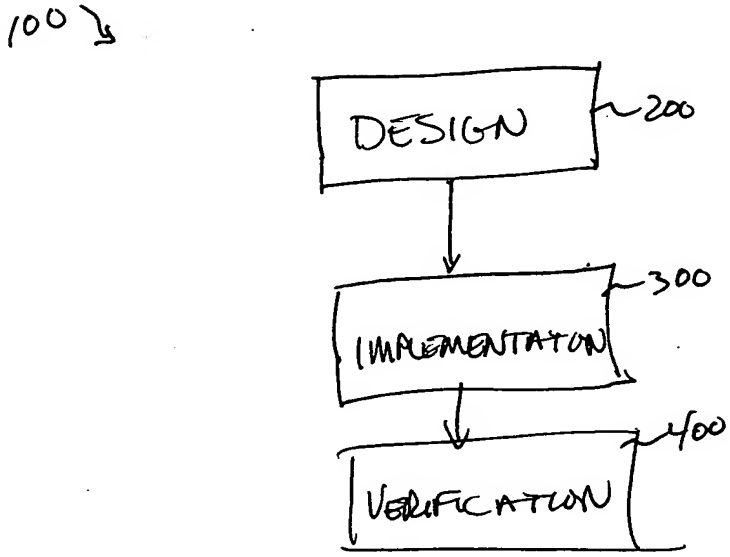

FIG. 1

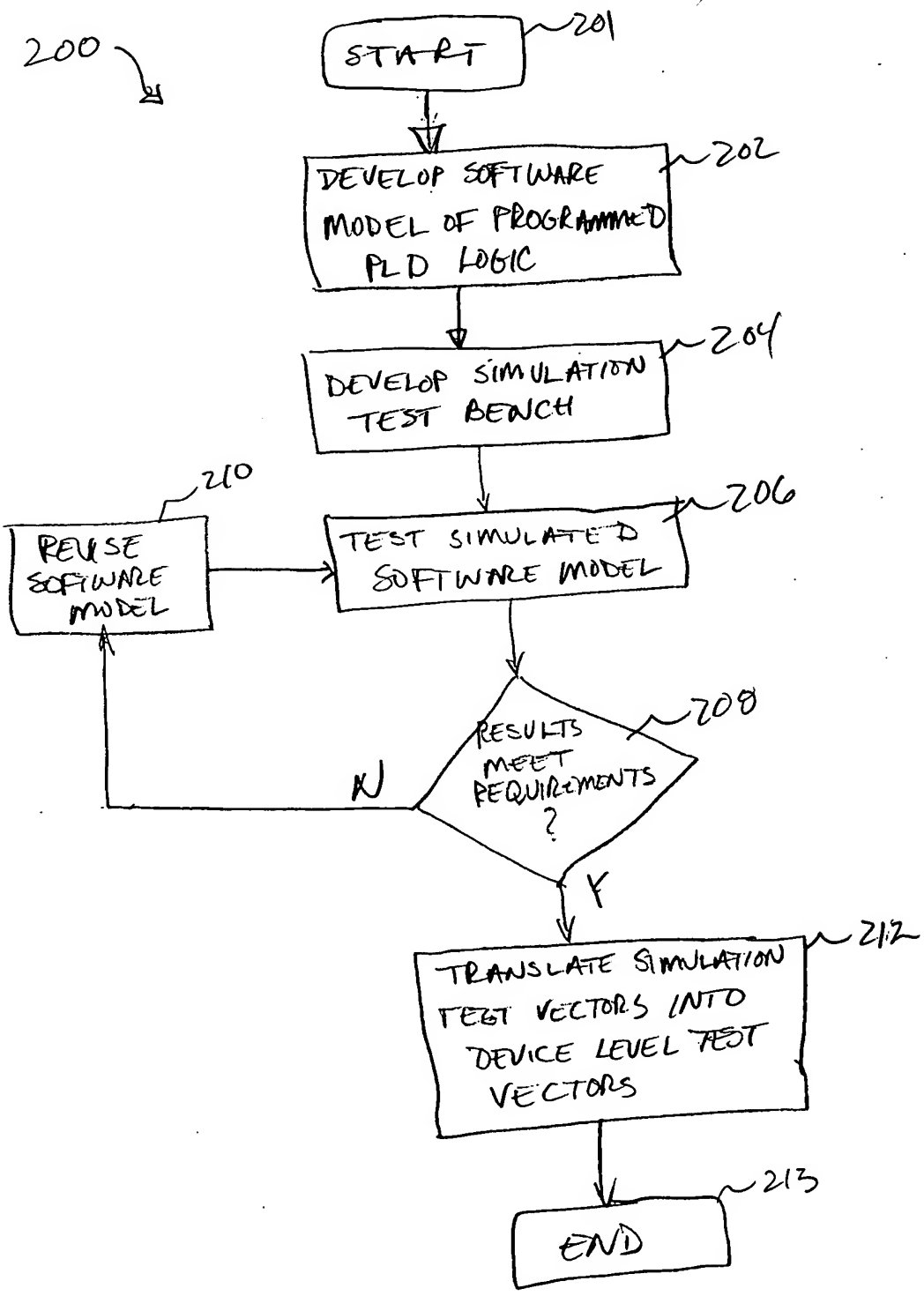
200
START
201
DEVELOP SOFTWARE MODEL OF PROGRAMMED PLD LOGIC
202
DEVELOP SIMULATION TEST BENCH
204
TEST SIMULATED SOFTWARE MODEL
206
RESULTS MEET REQUIREMENTS ?
208
N
Y
REVISE SOFTWARE MODEL
210
TRANSLATE SIMULATION TEST VECTORS INTO DEVICE LEVEL TEST VECTORS
212
END
213

FIG. 2

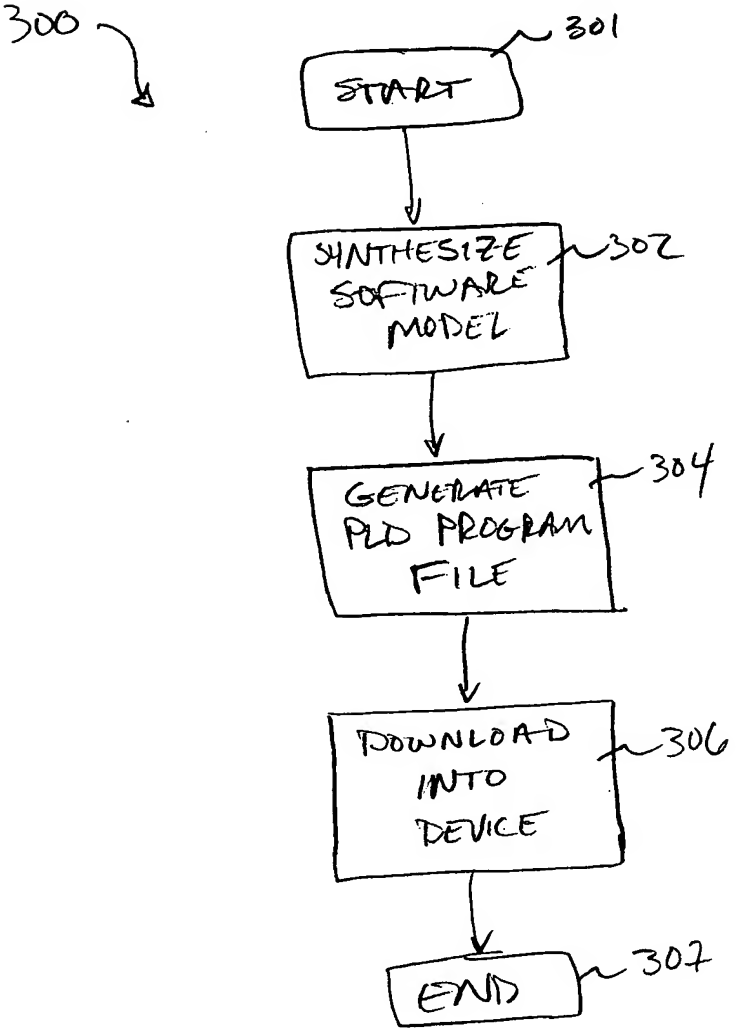
300
301
START
SYNTHESIZE SOFTWARE MODEL
302
GENERATE PLD PROGRAM FILE
304
DOWNLOAD INTO DEVICE
306
END
307

FIG. 3

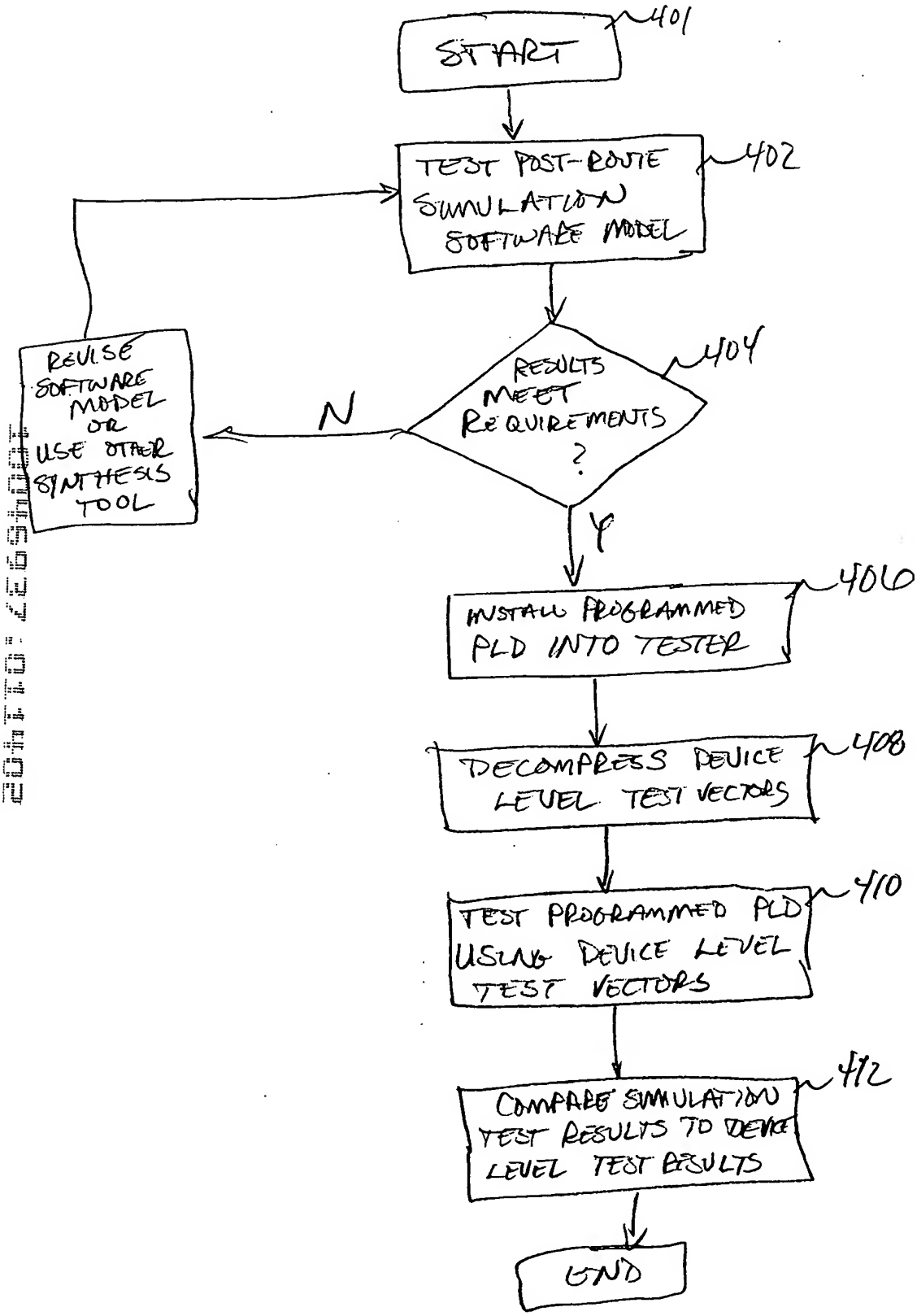
START
401
TEST POST-ROUTE SIMULATION SOFTWARE MODEL
402
RESULTS MEET REQUIREMENTS ?
404
N
REVISE SOFTWARE MODEL OR USE OTHER SYNTHESIS TOOL
Y
INSTALL PROGRAMMED PLD INTO TESTER
406
DECOMPRESS DEVICE LEVEL TEST VECTORS
408
TEST PROGRAMMED PLD USING DEVICE LEVEL TEST VECTORS
410
COMPARE SIMULATION TEST RESULTS TO DEVICE LEVEL TEST RESULTS
412
END

Fig. 4

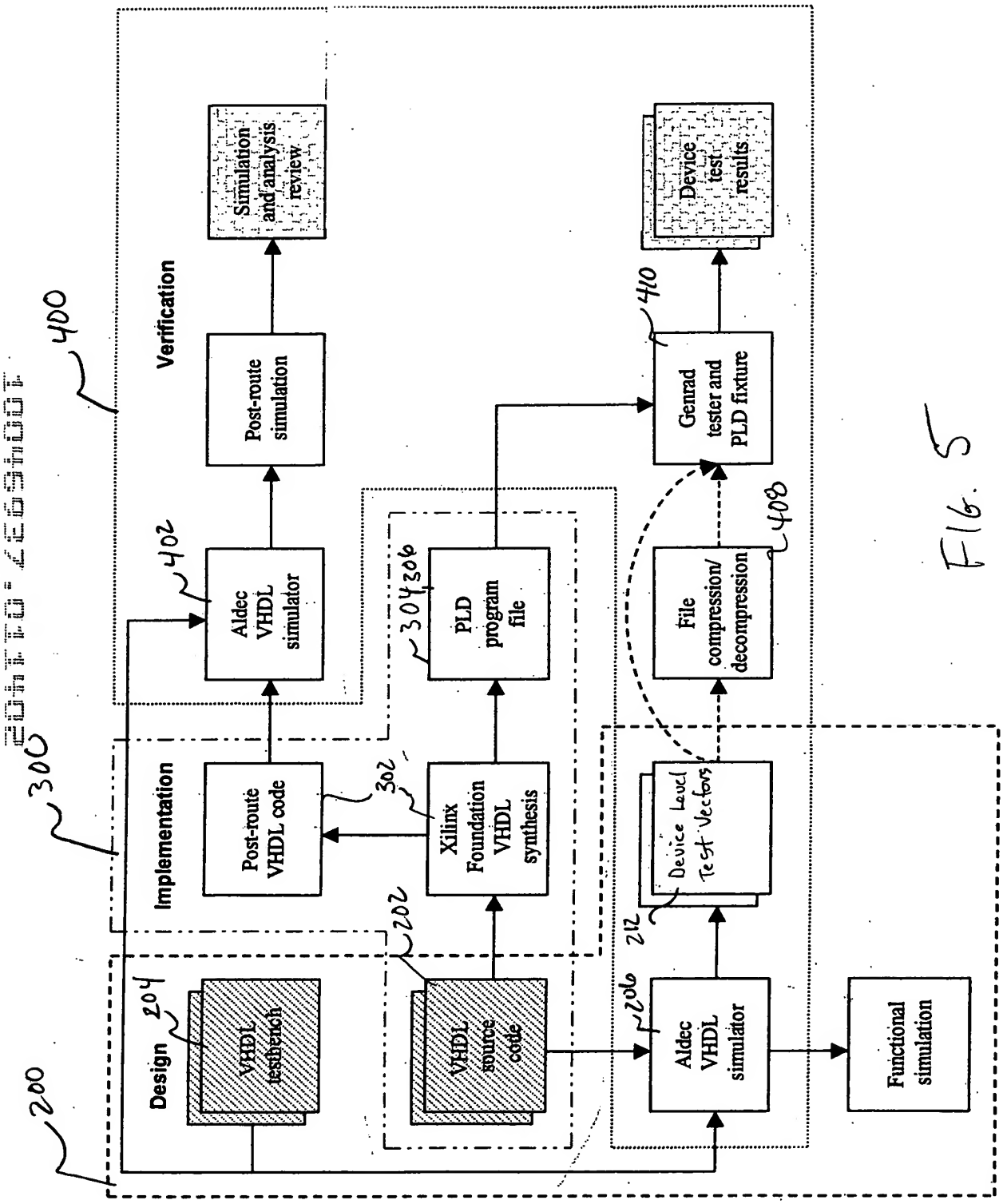
200
Design
204
VHDL testbench
202
VHDL source code
206
Aldec VHDL simulator
Functional simulation
212
Device Level Test Vectors
File compression/ decompression
408
Genrad tester and PLD fixture
410
Device test results
300
Implementation
Post-route VHDL code
302
Xilinx Foundation VHDL synthesis
304 306
PLD program file
Verification
400
Aldec VHDL simulator
402
Post-route simulation
Simulation and analysis review

FIG. 5

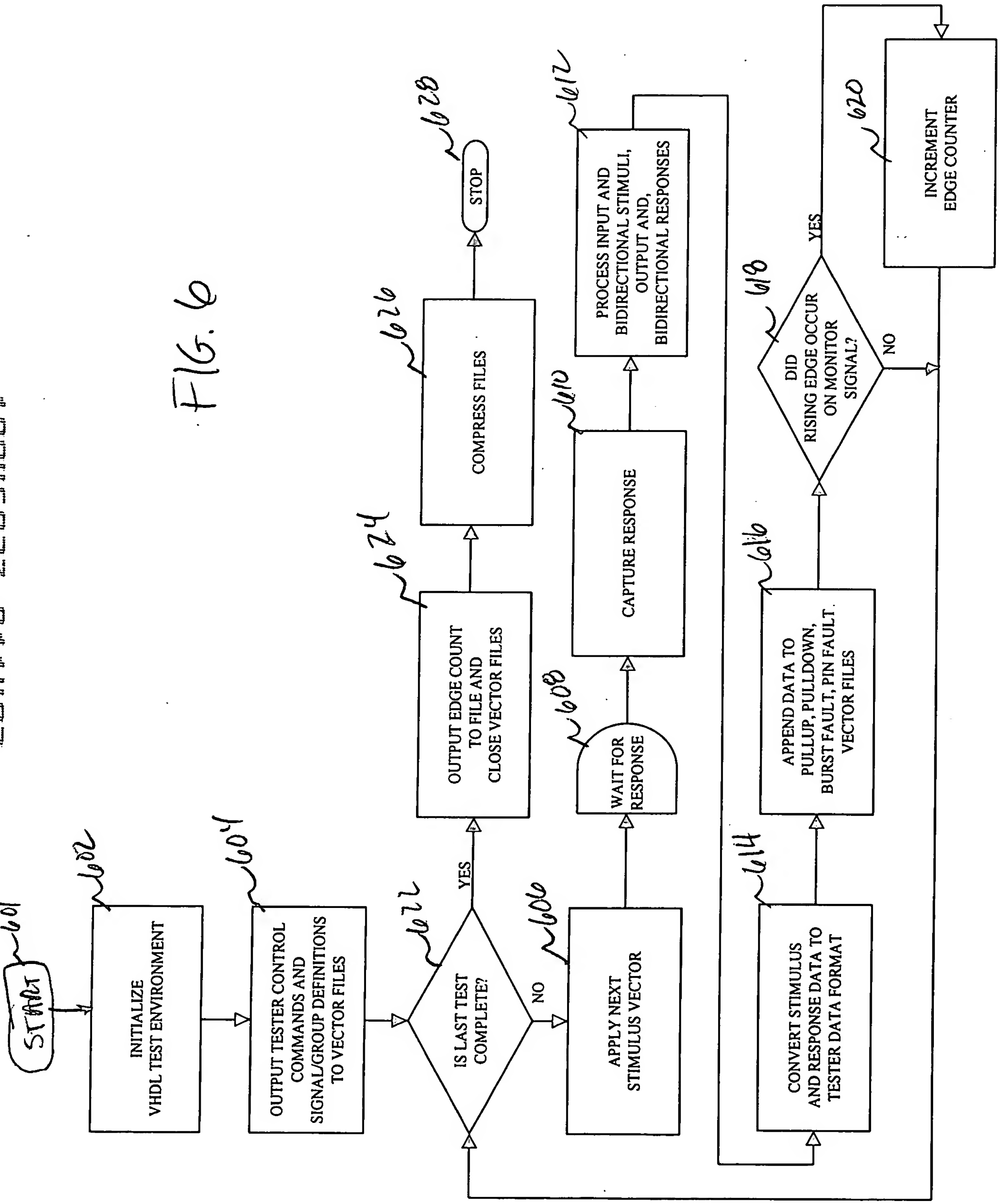
START
601
INITIALIZE VHDL TEST ENVIRONMENT
602
OUTPUT TESTER CONTROL COMMANDS AND SIGNAL/GROUP DEFINITIONS TO VECTOR FILES
604
IS LAST TEST COMPLETE?
622
YES
NO
APPLY NEXT STIMULUS VECTOR
606
WAIT FOR RESPONSE
608
CAPTURE RESPONSE
610
PROCESS INPUT AND BIDIRECTIONAL STIMULI, OUTPUT AND, BIDIRECTIONAL RESPONSES
612
CONVERT STIMULUS AND RESPONSE DATA TO TESTER DATA FORMAT
614
APPEND DATA TO PULLUP, PULLDOWN, BURST FAULT, PIN FAULT VECTOR FILES
616
DID RISING EDGE OCCUR ON MONITOR SIGNAL?
618
YES
NO
INCREMENT EDGE COUNTER
620
OUTPUT EDGE COUNT TO FILE AND CLOSE VECTOR FILES
624
COMPRESS FILES
626
STOP
628

FIG. 6